UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte TONGBI JIANG and EDWARD A. SCHROCK

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Appeal No. 2004-2144
Application No. 09/483,712

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ON BRIEF

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Before WALTZ, DELMENDO, and PAWLIKOWSKI, Administrative Patent Judges.

WALTZ, Administrative Patent Judge.

**DECISION ON APPEAL**

This is a decision on an appeal from the primary examiner's final rejection of claims 1 through 20. The remaining claims in this application are claims 21 through 29, which stand withdrawn from further consideration as directed to a non-elected invention (Brief, page 2). We have jurisdiction pursuant to 35 U.S.C. § 134.

According to appellants, the invention is directed to chip-scale semiconductor packages in a ball grid array configuration using a lead frame as an interposer (Brief, page 3). A further

understanding of the invention may be gleaned from representative independent claim 1, as reproduced below:

1. A chip-scale package comprising:

a semiconductor die having an active surface having at least one bond pad thereon;

at least one conductive trace spaced from said at least one bond pad and having an upper surface and a lower surface, the lower surface of said at least one conductive trace substantially non-conductively attached to a portion of the active surface of said semiconductor die;

at least one discrete conductive bond member connecting the at least one conductive trace to the at least one bond pad on the active surface of said semiconductor die;

at least one carrier bond attached to the upper surface of the at least one conductive trace; and

an encapsulant material encapsulating said semiconductor die, the at least one conductive trace, the at least one discrete conductive bond and a portion of the at least one carrier bond, the at least one carrier bond having another portion extending beyond said encapsulant material.

Appellants state that the claims do not stand or fall together (Brief, page 4), contrary to the examiner's statement (Answer, page 3, ¶(7); see the Reply Brief, page 2). Since appellants provide reasonably specific, substantive arguments for the patentability of individual claims 3, 6, 11, 12 and 14 (Brief, page 9), we consider these claims separately while the remaining claims stand or fall together. See 37 CFR

§ 1.192(c)(7)(2002); *In re McDaniel*, 293 F.3d 1379, 1383, 63 USPQ2d 1462, 1465 (Fed. Cir. 2002).

The examiner has relied upon the following references as evidence of obviousness:

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| Lee et al. (Lee) | 5,894,107 | Apr. 13, 1999 |
| Farnworth | 6,147,413 | Nov. 14, 2000 (filed Aug. 7, 1997) |

The claims on appeal stand rejected under 35 U.S.C. § 103(a) as unpatentable over Farnworth in view of Lee (Answer, page 3). We *affirm* the examiner's rejection on appeal essentially for the reasons stated in the Answer and those reasons set forth below.

**OPINION**

The examiner finds that Farnworth discloses a chip scale package comprising a semiconductor die (1004) having an active surface, a plurality of bond pads (1002), with the lower surface of a dielectric element (1006) attached to a portion of the active surface of the die (Answer, page 4). The examiner also finds that the lower surface of a plurality of conductive traces (1016) is attached to the upper surface of the dielectric element (1006), with conductive bond members connecting each conductive trace to the bond pads (*id.*). The examiner further finds that carrier bonds (1032) are disposed on an upper surface of the conductive trace and an encapsulating material (1018) covers

portions of the die, the dielectric element, the conductive traces, the bond members and the carrier bonds (*id.*). The examiner recognizes that Farnworth discloses all of the claimed elements except the discrete conductive bond connecting the conductive trace to the bond pad (*id.*). Therefore the examiner applies Lee to show a similar chip-size package[1] in which a conductive trace is spaced from a bond pad, with a discrete conductive bond in the form of a wire connecting the conductive trace to a bond pad formed on the surface of a semiconductor chip (*id.*).[2] From these findings, the examiner concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ the discrete conductive

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[1]In the event of further or continuing prosecution of this application, the examiner and appellants should consider whether Lee alone discloses structures meeting the claimed limitations (i.e., see Figures 9-11).

[2]The examiner states that the use of discrete electrical bonds (lead or bond wires) was "notoriously well known" in the art, as evidenced by appellants' Figure 1 which is listed as "Prior Art" (Answer, page 5). We also note that Figure 1 of Lee is labeled as "PRIOR ART" and contains bond wires 80 connecting bonding pad 74 to lead 76. It is axiomatic that admitted prior art in an applicant's specification may be used in determining the patentability of a claimed invention (*In re Nomiya,* 509 F.2d 566, 570-71, 184 USPQ 607, 611-12 (CCPA 1975); and that consideration of the prior art cited by the examiner may include consideration of the admitted prior art found in an applicant's specification (*In re Davis,* 305 F.2d 501, 503, 134 USPQ 256, 258 (CCPA 1962); *cf., In re Hedges,* 783 F.2d 1038, 1039-40, 228 USPQ 685, 686 (Fed. Cir. 1986)).

bonds in the form of wires in the configuration of Farnworth for the benefits taught by Lee, namely to provide the advantage of smaller packages, better electrical performance and higher package density (Answer, page 5). We agree.

Appellants argue that the fact that bond wires such as those taught by Lee are known in the art does not mean that bond wires may be incorporated into the structure disclosed by Farnworth (Brief, page 6). Appellants argue that, due to the differences in structure and scale between the repattern traces of Farnworth and the wires of Lee, there is no support for the examiner's proposed modification (Brief, page 7). Appellants further argue that adding bond wires to the repattern structure of Farnworth would require an enlarged packaged size, would decrease electrical performance, and complicate the manufacturing process (Brief, pages 7-8; Reply Brief, pages 3-4). Appellants state that the negative impact of adding bond wires to the flip chip package in Farnworth is based on structural aspects of bond wires "which are widely documented and well known to those of ordinary skill in the art." Reply Brief, page 3.

Appellants' arguments are not persuasive. The arguments of appellants' attorney cannot take the place of evidence lacking in the record. *See In re Scarborough,* 500 F.2d 560, 566, 182 USPQ

298, 302 (CCPA 1974); *In re Lindner,* 457 F.2d 506, 508, 173 USPQ 356, 358 (CCPA 1972). Appellants have not, on this record, substantiated their argument that the negative impact of adding bond wires is "widely documented and well known" in the art. In contrast, the examiner has shown evidence of the similarity in structures and purpose of Farnworth and Lee, as well as motivation to modify the structure of Farnworth, i.e., the advantages taught by Lee for the lead on chip (LOC) package (Answer, paragraph bridging pages 4-5 and pages 6-7). *See In re Mayne,* 104 F.3d 1339, 1342, 41 USPQ2d 1451, 1454 (Fed. Cir. 1997)("When relying on numerous references or a modification of prior art, it is incumbent upon the examiner to identify some suggestion to combine references or make the modification. [Citations omitted]."). We determine that the examiner has met the initial burden of establishing a case of *prima facie* obviousness for reasons discussed above. We note that appellants have not challenged or contested the examiner's showing of motivation or suggestion of modification (i.e., the advantages taught by Lee). Appellants have only presented unsupported arguments concerning the negative impact of the proposed modification.

Appellants argue that the combination of Farnworth and Lee does not teach or suggest the claim limitations of claims 3, 6, 11, 12 and 14 (Brief, page 9). This argument is not persuasive since the applied references disclose the adhesive-coated polyimide tape recited in claim 3 on appeal (e.g., see Lee, col. 4, ll. 60-63), the lead fingers of the conductive traces as recited in claim 6 on appeal (e.g., see Farnworth, col. 4, ll. 33-38), and the thermocompression bonds of claims 11 and 12 on appeal (e.g., see Lee, col. 4, ll. 65-67). Furthermore, Lee teaches external connection means exposed for electrical connection to the external interconnections (col. 5, ll. 21-24), and thus would have suggested any conductive element such as a conductive polymer as recited in claim 14 on appeal that would suffice for the external connection.

For the foregoing reasons and those stated in the Answer, we determine that the examiner has established a *prima facie* case of obviousness in view of the reference evidence. Based on the totality of the record, including due consideration of appellants' arguments, we determine that the preponderance of evidence weighs most heavily in favor of obviousness within the meaning of section 103(a). *See In re Oetiker,* 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). Accordingly, we

affirm the examiner's rejection of claims 1 through 20 under 35 U.S.C. § 103(a) over Farnworth in view of Lee.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a)(iv)(effective Sep. 13, 2004; 69 Fed. Reg. 49960 (Aug. 12, 2004); 1286 Off. Gaz. Pat. Office 21 (Sep. 7, 2004)).

**AFFIRMED**

Thomas A. Waltz
Administrative Patent Judge )
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Romulo H. Delmendo ) BOARD OF PATENT
Administrative Patent Judge ) APPEALS
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